In the Claims:

Applicant has submitted a new complete claim set indicating marked-up claims with insertions and deletions indicated by underlining and strikeouts or double-bracketing, respectively.

Claims 1, 7, and 10 are amended. Claims 2, 6, 11 and 18 are cancelled without prejudice. New claim 25 is added.

1. (Currently amended) An analog to digital converter, the converter comprising:
N input channels, where N is a positive integer; a converter for producing a digital representation of an analog signal supplied to the converter; ~~and~~ a multiplexer, and a sequencer for controlling the operation of the multiplexer, and wherein in a first mode of operation the sequencer is responsive to an N bit control word, wherein portions of the control word are associated with individual ones of the channels and define whether the associated channel is selected for conversion and wherein any one or more of the channels can be converted in sequence in response to ~~a user command~~ the control word, the unselected channels being skipped, such that the time required to convert the sequence of channels defined in the control word is proportional to the number of channels selected by the user in the control word, and wherein the N bit control word can be modified during the conversion of any one of the channels.

2. (DELETED)

3. (Original) An analog to digital converter as claimed in claim 1, wherein within the sequence the channels are converted in order of channel number and any given channel is only converted once.

4. (Original) An analog to digital converter as claimed in claim 1, further comprising a controller for controlling operation of the converter, and wherein user instructions concerning the

sequence of channels to be converted are written to the controller via a digital interface.

5. (Original) An analog to digital converter as claimed in claim 1, wherein the digital representation of the analog signal is associated with the identity of the channel converted.

6. (DELETED)

7. (Currently amended) An analog to digital converter as claimed in claim [[6]] 1, wherein the control word is N bits long with each individual bit being associated with a respective one of the channels.

8. (Original) An analog to digital converter as claimed in claim 7, in which an ith bit is associated with an ith channel, where i is an integer in the range one to N.

9. (Original) An analog to digital converter as claimed in claim 7, wherein the control word is held in a special purpose register, and outputs of the register are provided to respective inputs of the sequencer

10. (Currently amended) An analog to digital converter as claimed in claim 9, wherein the sequencer includes a plurality of registers arranged so as to form a chain, and wherein each register has an output that can be in either a first state or a second state, and wherein, in use, one register is in the first state and each of the other registers is in the second state, and wherein response to a shift signal, the registers sequentially pass the first state along the chain, with each register corresponding to a non-selected channel effectively being by-passed.

11. (DELETED)

12. (Original) An analog to digital converter as claimed in claim 10, wherein each register comprises a latch having an input and an output and is responsive to a clock signal

provided at a clock input such that, in response to a predetermined event in the clock signal, the signal at the input is latched by the register and a representation of that signal is provided at the output thereof if the register is selected by a select signal.

13. (Original) An analog to digital converter as claimed in claim 12, wherein each register comprises first and second logic elements, each logic element having an input, an output and a respective clock input, wherein the input of the first logic element serves as an input to the register, the output of the first element is connected to the input of the second element and the output of the second element serves as the output of the register, and wherein the respective clocks of the logic elements one normally driven in anti phase such that when one of the clocks is in a first state, the other clock is in a second state, and vice versa.

14. (Original) An analog to digital converter as claimed in claim 13, wherein, when the clock is in the first state the output of the logic element tracks the input thereto.

15. (Original) An analog to digital converter as claimed in claim 14, wherein each register is further responsive to a respective channel select signal and wherein, in the event that the channel is not selected, the clock signal to the first and second logic elements is held in the first state.

16. (Original) An analog to digital converter as claimed in claim 15, in which when not selected, the respective register acts as a buffer.

17. (Original) An analog to digital converter as claimed in claim 10, in which the output of each register is gated such that only the outputs of selected ones of the registers corresponding to selected channels can be propagated to the multiplexer.

18. (DELETED)

19. (Currently Amended) A circuit comprising a plurality of latches arranged such that the output of latch is provided to the input of a subsequent latch, and wherein in a first mode of operation a latch selected by a respective latch mode control signal is arranged to latch a signal received at its input in response to a latch signal, and in a second mode of operation the input at the latch is transferred directly to its output irrespective of the state of the latch mode control signal.

20. (Original) A circuit as claimed in claim 19, wherein the circuit is arranged to sequentially shift a logic "one" through the series of latches, whereby only selected latches as selected by the latch mode control signal participate in the shifting process.

21. (Original) A circuit as claimed in claim 19, wherein the circuit is arranged to sequentially shift a logic "one" through a series of latches, whereby unselected latches as defined by a latch mode control signal are effectively bypassed or act as buffers.

22. (Original) A circuit as claimed in claim 19, wherein the circuit is arranged to sequentially shift a logic "zero" through the series of latches, whereby only selected latches as selected by the latch mode control signal participate in the shifting process.

23. (Original) A circuit as claimed in claim 19, wherein the circuit is arranged to sequentially shift a logic "zero" through a series of latches, whereby unselected latches as defined by a latch mode control signal are effectively bypassed or act as buffers.

24. (Original) A circuit as claimed in claim 19, wherein the outputs of the latches are further gated such that only the outputs of selected latches can be output.

25. (NEW) A latch circuit wherein a first mode the circuit latches an input signal an in a second mode the circuit directly propagates a signal from an input of the latch circuit to an output of the latch circuit, the latch circuit comprising a first latch having an input forming the

input of the latch circuit and having an output connected to the input of a second latch, which has an output acting as the output of the latch circuit, and wherein the first and second latches have respective clock inputs and the configuration of each latch is such that if its clock is at a first value then the signal at the input of the latch propagates to the output of the latch, and if it is at a second value then each latch latches its input, and wherein a clock signal to the latches is gated by a control signal such that if the control signal selects the first mode of operation the first and second latches receive their clock signals in antiphase, and if the control signal selects the second mode of operation each latch has its clock held at the first value.